FILE 'REGISTRY' ENTERED AT 15:42:18 ON 13 SEP 2002
L1 1 S NI SI/MF
L2 1 S SILICON NITRIDE/CN
L3 784 S N SI/MF OR N.SI/MF OR N SI/ELF
L4 784 S N SI/ELF
L5 2 S SILICON OXYNITRIDE/CN
L6 334 S (SI AND O AND N)/ELS AND 3/ELC.SUB
L7 2 S TANTALUM NITRIDE/CN
L8 121 S N.TA/MF OR N TA/MF
L9 2 S TITANIUM NITRIDE/CN
L10 264 S N.TI/MF OR N TI/MF
L11 1 S TUNGSTEN/CN
L12 1 S ALUMINUM/CN

FILE 'REGISTRY' ENTERED AT 16:02:14 ON 13 SEP 2002

FILE 'HCAPLUS' ENTERED AT 16:05:34 ON 13 SEP 2002
L13 11777 S THIN()FILM()TRANSISTOR OR TFT
L14 1136411 S LIGHT()EMITTING OR DIODE OR LIGHT OR LED OR LUMINESCENCE OR E
L15 218865 S TIN OR TAN OR (TATANIUM OR TANTALUM)(N)(NITRIDE) OR TANTALUM(
L16 1518107 S TUNGSTEN OR W OR AL OR ALUMINUM OR ALUMINIUM
L17 72932 S (SILICON OR SI)()(NITRIDE) OR (SILICON OR SI)()(OXYNITRIDE)
L18 1419 S L13 AND L14
L19 333 S L18 AND (L1-12 OR L15 OR L16 OR L17)
L20 6 S L19 AND N()TYPE
L21 1 S L19 AND N()CHANNEL
L22 74 S L19 AND GATE()ELECTRODE
L23 69 S (L22 OR L21) NOT L20

L20 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:936068 HCAPLUS
DN 136:45808
TI **Light emitting** device and manufacturing method thereof
IN Yamazaki, Shunpei; Fukunaga, Takeshi; Koyama, Jun; Inukai, Kazutaka
PA Japan
SO U.S. Pat. Appl. Publ., 37 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001055841	A1	20011227	US 2001-832867	20010412
JP 2002057162	A2	20020222	JP 2001-118527	20010417
PRAI JP 2000-115699	A	20000417		

AB **Light emitting** devices are described comprising an n-channel **TFT** which may be a driver circuit and a **light emitting** element in each of pixels, the n-channel **TFT** comprising: an active layer including: a channel forming region; an **n-type** impurity region adjacent to the channel forming region; an **n-type** impurity region adjacent to the **n-type** impurity region; and an **n-type** impurity region adjacent to the **n-type** impurity region; a gate insulating layer provided over the active layer; and a gate electrode provided over the gate insulating layer including: a first gate electrode provided over the gate insulating layer; and a second gate electrode provided over the first gate, wherein the first gate electrode overlaps the channel forming region and the **n-type** impurity region (c) with the gate insulating layer therebetween, and wherein the second gate electrode overlaps the channel forming region with the gate insulating layer therebetween. Fabrication methods of the **light emitting** devices also described. Application of the **light emitting** devices in electronic devices is noted.

L20 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:703396 HCAPLUS
DN 129:324852
TI Fabricating a **thin-film transistor** for a liquid-crystal display device
IN Seo, Seong Moh
PA LG Electronics Inc., S. Korea
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5827760	A	19981027	US 1997-798826	19970212
PRAI KR 1996-3288		19960212		

AB A **thin-film transistor** is fabricated by introducing a dopant into an In Sn oxide layer or a gate insulating layer by an ion shower doping technique. An a-Si semiconductor layer is then deposited on the surface of the substrate and subjected to a single

exposure of laser **light**. The laser exposure or annealing diffuses dopant into the semiconductor layer and activates the dopant to form an ohmic layer of **n-type** or p-type polysilicon, and an intrinsic polysilicon layer. A metal layer and an In Sn oxide layer are formed to the side of a gate electrode to maintain an elec. connection even if a break is formed in the data bus line.

L20 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:180772 HCAPLUS
DN 120:180772
TI Manufacture of **thin film transistor**
IN Takahama, Manabu; Katayama, Mikio; Kondo, Naofumi; Kataoka, Yoshiharu; Nakazawa, Kyoshi; Myanochi, Makoto
PA Sharp Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05304170	A2	19931116	JP 1992-108081	19920427

AB The title transistor is manufd. by a process including following successive steps; (1) successively depositing a **light**-shielding gate electrode, a transparent gate insulating film, a transparent channel semiconductor film, and a transparent **n+-type** semiconductor film on a transparent elec. insulating substrate, (2) forming a neg.-working photoresist film on the **n+-type** semiconductor film, (3) irradiating from the substrate side by using the gate electrode as a photomask to leave nonirradiated part of narrower width than the gate electrode, (4) removing the nonirradiated part, (5) etching over the resist film to sep. the **n+-type** semiconductor film, and (6) forming source electrode and drain electrode on the sepd. part. The resulting small-size **TFT** is useful for switching device in matrix display device.

L20 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:596095 HCAPLUS
DN 115:196095
TI Manufacture of **thin-film transistors**
IN Yoshida, Mamoru; Nobori, Masaharu; Nomoto, Tsutomu
PA Oki Electric Industry Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 03076231	A2	19910402	JP 1989-212607	19890818

AB The process includes: (a) forming a gate electrode from a metal on a transparent insulator substrate, where the metal can obtain an insulator cover by anodization; (b) depositing an **n-type** photoresist on the whole surface; (c) exposing the photoresist to **light** from the bottom side of the substrate; and (d) developing the photoresist to remove its unexposed part on the gate electrode. The steps are followed by: (e) forming a 1st gate insulator layer by anodizing

the gate surface; (f) removing the photoresist; (g) forming an image-element electrode on the substrate; and (h) forming a 2nd gate insulator layer, a semiconductor active layer, an ohmic contact layer, and source and drain electrodes on the 1st gate insulator layer.

L20 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:596094 HCAPLUS
DN 115:196094
TI Manufacture of **thin-film transistors** for display devices
IN Yoshida, Mamoru; Nishiki, Tamahiko; Koizumi, Masumi; Shimizu, Mari
PA Oki Electric Industry Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 03076232	A2	19910402	JP 1989-212608	19890818
JP 2938895	B2	19990825		

AB The process includes: (a) forming a gate electrode from a metal on a transparent insulator substrate, where the metal can obtain an insulator cover by anodization; (b) depositing an **n-type** photosensitive polyimide on the whole surface; (c) exposing the polyimide to **light** from the bottom side of the substrate; and (d) developing the polyimide to remove its unexposed part on the gate electrode. The steps are followed by: (e) forming a 1st gate insulator layer by anodizing the gate surface; (f) hardening the polyimide by heating; (g) forming a 2nd gate insulator layer on the polyimide and the 1st gate insulator layer; and (h) forming a semiconductor active layer, source and drain electrodes, and an image-element electrode on the 2nd gate insulator layer.

L20 ANSWER 6 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1965:40901 HCAPLUS
DN 62:40901
OREF 62:7215d-e
TI Thin-film active elements. I. Metal-base transistor constructed on an evaporated tantalum film
AU Numba, Susumu
CS Inst. Phys. Chem. Res., Tokyo
SO Rika Gaku Kenkyusho Hokoku (1964), 40(2), 92-106
DT Journal
LA Unavailable
AB To make a metal-base **thin-film transistor**, the elec. properties of a Ta film deposited by the electron-beam heating method were measured. The characteristics of a Ta-Ta2O5-**Al diode** were measured at 77-373.degree.K. to study the mechanism of current flow. The Schottky current is dominant at room temp. and the barrier height of Ta-Ta2O5-**Al** is .apprx.1.1 ev. Characteristics of an **Al**-Ta2O5-Ta-**n-type** Si **thin-film transistor** were also measured.

L23 ANSWER 1 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:540206 HCAPLUS
DN 137:101514
TI Method of manufacturing **TFT** for liquid crystal displays using gettering
IN Yamazaki, Shunpei; Murakami, Satoshi; Ohnuma, Hideto; Nakamura, Osamu; Tanaka, Koichiro; Arai, Yasuyuki
PA Japan
SO U.S. Pat. Appl. Publ., 49 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002094613	A1	20020718	US 2002-34498	20020103
PRAI JP 2001-10858	A	20010118		

AB The present invention was characterized in that gettering was performed such that impurity regions to which a noble gas element is added are formed in a semiconductor film and the metallic element included in the semiconductor film is segregated into the impurity regions by laser annealing. Also, a reflector is provided under a substrate on which a semiconductor film is formed. When laser **light** transmitted through the semiconductor film substrate is irradiated from the front side of the substrate, the laser beam is reflected by the reflector and thus the laser **light** can be irradiated to the semiconductor film from the read side thereof. Laser **light** can be also irradiated to low concn. impurity regions overlapped with a portion the **gate electrode**. Thus, an effective energy d. in the semiconductor film is increased to thereby effect recovery of crystallinity and activation of the impurity element.

L23 ANSWER 2 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:486592 HCAPLUS
DN 137:54770
TI **Thin-film transistor** for **TFT** array, liquid crystal display, and **electroluminescence** display, and manufacture thereof
IN Kawakita, Tetsuro
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2002185009	A2	20020628	JP 2000-384842	20001219

AB The **thin-film transistor** comprises an insulating subbing layer, a semiconductor layer having a channel region and a source.cntdot.drain region, a TEOS gate insulating film, and a Mo/**W** alloy **gate electrode** formed on an insulating substrate. The process comprises a degasing step effected after forming the semiconductor layer, the gate insulating film, and the **gate electrode** to remove impurities, wherein a peak of an emission profile of H2, H2O, and O2 is set at .gtoreq.600.degree.. A **TFT**

array, a liq. crystal display, and an **electroluminescence** display using above **TFTs** are also claimed. The process suppressed an interfacial reaction between the gate insulating film and the **gate electrode**, thereby increasing the BT resistance.

L23 ANSWER 3 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:486584 HCAPLUS
DN 137:40373
TI Manufacture of thin-film semiconductor devices
IN Tsugiroku, Hiroaki; Miyasaka, Mitsutoshi; Ogawa, Tetsuya; Tokioka, Hidetada
PA Seiko Epson Corp., Japan; Mitsubishi Electric Corp.
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2002184996	A2	20020628	JP 2000-378960	20001213

AB The process includes: (a) forming elec. conductive films (e.g., Ta) on substrates, (b) patterning the conductive films into **TFT** bottom electrodes, (c) forming insulator films on the electrodes, (d) forming source contact holes and bottom electrode contact holes in the insulator films, (e) forming semiconductor films on the insulator films as well as in the contact holes, (f) applying **light** from the semiconductor film side to improve the crystallinity of the semiconductor films, (g) patterning the semiconductor films, (h) forming gate insulator films on the patterned semiconductor films, (i) forming **gate electrodes** on the gate insulator films, and (j) implanting impurities in the semiconductor films to form source and drain regions. Thin-film semiconductor devices thus manufd. have restricted parasitic bipolar effect.

L23 ANSWER 4 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:429487 HCAPLUS
DN 137:14409
TI Method for fabricating **thin film transistor** including crystalline silicon active layer
IN Lee, Seok Woon; Joo, Seung Ki
PA Pt Plus Co. Ltd., S. Korea
SO U.S. Pat. Appl. Publ., 27 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002068392	A1	20020606	US 2001-826439	20010404
JP 2002208599	A2	20020726	JP 2001-366065	20011130
PRAI KR 2000-72592	A	20001201		

AB The present invention relates to a **TFT** used for liq. crystal display (LCD) and org. **light emitting diode** (OLED). More particularly, the present invention relates to a **TFT** including a cryst. silicon active layer providing the source, drain, and channel regions of the **TFT**, and to a method for fabricating a

TFT including the cryst. silicon active layer. The method for fabricating a **TFT** includes a cryst. Si active layer, in which the metal which induced the crystn. of the active layer is offset from a **gate electrode** using a mask used to form a lightly doped drain (LDD) region or an offset junction region in the active layer. The **TFT** includes a Si active layer crystd. by crystn. inducing metal and a **gate electrode**, and has an LDD region or an offset junction region formed in the vicinity of the channel region. The method for fabricating the **TFT** forms a metal offset region without using an addnl. photoresist forming process, and forms a LDD region by conducting a low d. doping in the metal offset region. As a result, a transistor made according to the present invention has low leakage current in its off-state, and has stable elec. characteristics in its on-state.

L23 ANSWER 5 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:407317 HCAPLUS
DN 136:394434
TI Fabrication of thin-film semiconductor devices for dopant activation by rapid heating
IN Kunii, Masafumi
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 16 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2002158358	A2	20020531	JP 2000-352712	20001120

AB The fabrication of a pl. no. of top-gate **TFTs** on a substrate involves (1) forming a cryst. semiconductor thin film on the substrate, (2) etching a single semiconductor layer to sep. into isolated semiconductor regions, (3) coating over each isolated semiconductor region with a gate insulator film, (4) providing a **gate electrode** on each gate insulator film, (5) doping into the semiconductor regions to give source/drain regions without deterioration of the semiconductor crystal, and (6) lamp-annealing for rapid thermal activation (RTA) of the dopants in the component-isolated semiconductor thin films. The process makes possible for fabrication of top-gate polysilicon **TFTs** by RTA in manuf. of liq. crystal display devices and org. **electroluminescence** display devices.

L23 ANSWER 6 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:368854 HCAPLUS
DN 136:393036
TI **Light-emitting** devices with **light-emitting** element formed between insulating partition layers
IN Yamazaki, Shunpei
PA Japan
SO U.S. Pat. Appl. Publ., 24 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI US 2002056842 A1 20020516 US 2001-986425 20011108
JP 2002208477 A2 20020726 JP 2001-345439 20011109
PRAI JP 2000-342739 A 20001110
AB **Light-emitting** devices are described which comprise a first insulating layer of **silicon nitride** or **silicon oxynitride**; a second insulating layer of **silicon oxynitride** over the first insulating layer; a **thin film transistor** formed between the first and the second insulating layers, the **thin film transistor** having a semiconductor layer comprising silicon, a gate insulating film and a **gate electrode**; a third insulating layer made of **silicon nitride** or **silicon oxynitride** over the second insulating layer; a fourth insulating layer comprising carbon over the third insulating layer; a **light-emitting** element formed between the third and the fourth insulating layers, the **light emitting** element comprising an anode, an org. compd. layer, and a cathode comprising an alkali metal; and partition layers comprising an insulating material on the third insulating layer, where the **light emitting** element is formed between partition layers.

L23 ANSWER 7 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:313307 HCAPLUS
DN 136:332876
TI Liquid crystal display having **thin film transistor** and color-changeable layer and its manufacture
IN Matsumoto, Koichi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2002122884	A2	20020426	JP 2000-316714	20001017

AB The display comprises a transparent substrate with an active element, a transparent switching electrode, a color-changeable layer between the switching electrode and a **light** insulating **gate electrode** of the active element, and the coloring state is changed by applying elec. potential between the **gate electrode** and the switching electrode. Manuf. of the liq. crystal display equipped with **thin film transistor** and the color-changeable layer is also claimed. On-current and off leak-current of **TFT** are optimized.

L23 ANSWER 8 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:287496 HCAPLUS
DN 137:117493
TI Undergated **TFTS** with p + poly/**TiN** gates
AU Baker, Frank K.; McNelly, Thomas; Sitaram, A. R.; Nguyen, Bich Yen
CS USA
SO IP.com Journal (2002), 2(2), 148 (No. IPCOM000006678D), 28 Feb 2002
CODEN: IJPOBX; ISSN: 1533-0001
PB IP.com, Inc.
DT Journal; Patent
LA English

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	IP 6678D		20020228		
PRAI	IP 2002-6678D		20020228		

AB Static RAMS with densities of 16Mb or more will require polysilicon PMOS **thin-film transistor** (**TFT**) loads to control standby current, improve the soft error rate, overcome **diode** leakage problems, and allow supply voltage scaling. The most common implementation of the **TFT** load involves forming a pair of polysilicon **gate electrodes**, which attach the SRAM data storage nodes, and then forming polysilicon channels which run across the top of each **gate electrode**, sepd. from the underlying gates by only a thin **TFT** dielec. This is known as the undergated approach to **TFT** fabrication. The technique described below uses **TiN** and p+ doped polysilicon to form the **TFT gate electrodes**. This choice of materials provides optimum interconnection between the various portions of the **TFT** load devices, without compromising the quality of the **TFT** dielec.

L23 ANSWER 9 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:119777 HCAPLUS
DN 136:176500
TI Manufacture of **light-emitting** devices
IN Yamazaki, Shunpei; Fukunaga, Kenji; Koyama, Jun; Inukai, Kazutaka
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 25 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002050633	A2	20020215	JP 2001-118926	20010417
	US 2002048829	A1	20020425	US 2001-837324	20010419
PRAI	JP 2000-117436	A	20000419		

AB Photolithog. in manuf. of **TFTs** involves fewer steps. **TFT gate electrodes** consist of .gtoreq.2 elec. conductive layers, and have gradually wider length downward which is achieved by utilizing different etching rates of the layers. Impurity concns. in active layers are adjusted by controlling acceleration voltage applied during impurity addn.

L23 ANSWER 10 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:87441 HCAPLUS
DN 136:142717
TI **Thin film transistors** (**TFT**) in liquid crystal display devices for liquid crystal projector and method for manufacturing liquid crystal display devices using same
IN Matsushima, Yasuhiro
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 16 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	JP 2002033480	A2	20020131	JP 2000-212768	20000713

AB The title **TFT** has a first **gate electrode**, a first gate dielec. layer, a semiconductor layer, a second gate dielec. layer, and a second **gate electrode** on a substrate, wherein the semiconductor layer has a high impurity region, which includes a channel region, a source region, and a drain region and a low impurity region and wherein the first **gate electrode** is made of a **light**-blocking material and formed in a region corresponding to the channel region and the low impurity region. The **TFT** shows the good **light**-resistance and the increased on-state-current and withstand voltage of the source-drain and suitable for small mobile liq. crystal projectors.

L23 ANSWER 11 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:66961 HCAPLUS
DN 136:94429
TI Method of manufacturing a **thin film transistor**
IN In, Tae Hyung; Jo, Sang Gwon
PA Hyundai Electronics Ind. Co., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI KR 2000015174	A	20000315	KR 1998-34940	19980827

AB A method of manufg. a **thin film transistor** is provided to obtain a high mobility. A method of manufg. a **thin film transistor**(**TFT**) comprises the following steps: forming a **gate electrode** and prepg. a **light**-flooding substrate on which a gate insulation layer is entirely applied to coat the **gate electrode**; evapg. an amorphous Si layer on the gate insulation layer; patterning the amorphous Si layer and the gate insulation layer; forming **Si nitride** layer in a form of a pattern on the amorphous Si layer on the **gate electrode**; ion-injecting impurities into the amorphous Si layer by using the **Si nitride** layer as a ion-injecting mask; crystg. the amorphous Si layer corresponding to source/drain regions by performing a heat treatment process regarding the amorphous layer at the rear surface of the **light**-flooding substrate; eliminating the remaining metal layer having not reacted with the amorphous Si layer after the heat treatment process; forming a passivation layer having a contact hole for exposing the crystd. source/drain regions on the entire surface; and forming source/drain electrodes contacted with the source/drain regions on the passivation layer.

L23 ANSWER 12 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:868841 HCAPLUS
DN 136:14083
TI Fabrication of a semiconductor device with a source electrode, a drain electrode and a source bus
IN Hatta, Yoshihisa
PA Koninklijke Philips Electronics N.V., Neth.
SO PCT Int. Appl., 27 pp.

CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2001091172	A2	20011129	WO 2001-EP5261	20010508
WO 2001091172	A3	20020321		
W: CN, KR				
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR				
JP 2001332735	A2	20011130	JP 2000-151234	20000523
US 2002048863	A1	20020425	US 2001-861939	20010521
PRAI JP 2000-151234	A	20000523		

AB The invention provides a semiconductor device and a method for forming patterns in which the manufg. cost is reduced while the step coverage is improved. The ITO film and the MoCr film are dry-etched after having formed the ITO film and the MoCr film.

L23 ANSWER 13 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:840860 HCAPLUS
DN 135:365393
TI Thin film semiconductor devices and fabrication of **thin-film transistors** by laser-irradiation crystallization
IN Shimogaichi, Yasushi; Hayashi, Hisao; Kotoku, Masato
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001320056	A2	20011116	JP 2000-137557	20000510

AB The title fabrication of **TFTs** involves (1) forming a **gate electrode** on an insulative substrate, (2) forming a gate insulator film over the **gate electrode**, (3) depositing a semiconductor thin film on the gate insulator film, (4) crystg. the semiconductor thin film by laser irradn., and (5) doping the crystd. semiconductor thin film. The laser irradn. for the crystn. employs laser with its wavelength at .ltoreq.300 nm so as to give evenly distributed laser energy through the semiconductor film thickness direction.

L23 ANSWER 14 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:780521 HCAPLUS
DN 135:325088
TI Self-luminous device and electric machine using the same
IN Koyama, Jun; Inukai, Kazutaka
PA Sel Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 56 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI EP 1148553 A2 20011024 EP 2001-109522 20010417
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO
JP 2002006777 A2 20020111 JP 2001-117529 20010416
CN 1327270 A 20011219 CN 2001-116648 20010417
PRAI JP 2000-114592 A 20000417
AB Self-luminous (e.g., electroluminescent) elements are described in which a **gate electrode** of a current controlling **thin-film transistor** (**TFT**) formed on an insulator overlaps with a sep. semiconductor film with a gate insulating film sandwiched therebetween. Gray scale displays may be attained by a time division driving method in which the element provided in a pixel is controlled to emit **light** or not to emit **light** by means of time, thereby avoiding being affected by fluctuation in characteristic in current controlling **TFTs**. Other elec. devices incorporating the elements or displays are also described.

L23 ANSWER 15 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:581421 HCAPLUS
DN 135:160218
TI Semiconductor device and manufacturing method thereof
IN Yamazaki, Shunpei
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 40 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 1122794	A2	20010808	EP 2001-102321	20010201
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
US 2001040645	A1	20011115	US 2001-774388	20010130
JP 2001290439	A2	20011019	JP 2001-23509	20010131
CN 1312590	A	20010912	CN 2001-116881	20010201
PRAI JP 2000-24540	A	20000201		

AB Methods of manufg. semiconductor devices (e.g., electroluminescent displays) are described which entail forming a sepg. layer on a first substrate; forming an insulating film on the sepg. layer; forming **light-emitting** elements on the insulating film; attaching a fixing substrate to the **light-emitting** elements using a first adhesive layer; removing the sepg. layer by exposing it to a gas contg. halogen fluoride to sep. the first substrate; and attaching a second substrate on which color filters are provided to the insulating film using a second adhesive layer. Method of manufg. semiconductor devices (e.g. liq. crystal displays) are also described which entail forming a sepg. layer on a first substrate; forming an insulating film on the sepg. layer; forming an active layer, a gate insulating film, and **gate electrodes** on the insulating film; forming a first interlayer insulating film over the **gate electrodes**; forming wiring and pixel electrodes on the first interlayer insulating film; attaching a fixing substrate provided with an opposing electrode on the first substrate using a sealant; injecting a liq. crystal between the pixel electrodes and the opposing electrode; removing the sepg. layer by exposing the sepg. layer to a gas contg. halogen fluoride to sep. the first substrate; and attaching a second

substrate provided with color filters to the insulating film using an adhesive layer. Semiconductor devices are also described which comprise an adhesive layer on a substrate; an insulating film on the adhesive layer; and **light emitting** elements on the insulating film,wherein emitted from the **light emitting** elements is emitted through the substrate. Preferably, the substrate is a plastic substrate provided with color filters under the adhesive layer. Semiconductor devices comprising a first substrate comprising an org. material and having **thin-film transistors** (**TFTs**) provided thereon; a second substrate; and a liq. crystal material retained between the first and second substrates, wherein color filters are provided between the first substrate and the **TFTs**, .a black mask together with the color filters.

L23 ANSWER 16 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:566677 HCAPLUS
DN 135:129667
TI Thin-film display system
IN Takayama, Ichiro
PA TDK Corporation, Japan
SO U.S. Pat. Appl. Publ., 16 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001010374	A1	20010802	US 2000-740866	20001221
	JP 2001209331	A2	20010803	JP 2000-18659	20000127
PRAI	JP 2000-18659	A	20000127		

AB The invention relates to a thin film display system using thin film **light-emitting** devices such as org. **electroluminescence** devices. The system comprises on the same substrate ,a thin-film display device driven at a current for each pixel to emit **light** and a Si thin-film layer on which a circuit for driving the thin-film display device is formed. The display system further comprises a region where at least the thin-film display device and the Si thin-film layer overlap each other in a film thickness direction, so that a part of **light** emitted from the thin-film display device is taken out of that region.

L23 ANSWER 17 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:392118 HCAPLUS
DN 134:374163
TI **Thin film transistor** for an optical sensor for reflected **light**
IN Chang, Youn Gyoung; Kim, Jeong Hyun; Kim, Se June; Lee, Jae Kyun; Yi, Jong Hoon
PA LG Philips LCD Co. Ltd., S. Korea
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6239468	B1	20010529	US 1999-456389	19991208

PRAI KR 1998-54096 A 19981210
AB A sensor **TFT** includes a substrate, a **gate electrode** formed on the substrate, a semiconductor layer patterned on the insulating layer to generate an optical current using received **light**, source and drain electrodes formed on the semiconductor layer, the source and drain electrodes being spaced apart from each other, and a conductive channel defined by an area between the source and drain electrodes, wherein the conductive channel is not rectangular-shaped, such that the channel width is increased for a fixed channel length.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 18 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:338182 HCAPLUS
DN 134:346551
TI Electroluminescent display device
IN Yamazaki, Shunpei; Koyama, Jun
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 48 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1098290	A2	20010509	EP 2000-124155	20001107
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2001222256	A2	20010817	JP 2000-336454	20001102
PRAI	JP 1999-316935	A	19991108		
	JP 1999-337004	A	19991129		

AB Display devices capable of preventing a redn. of an elec. charge stored in a **gate electrode** of an **electroluminescence** driver **thin-film transistor** (**TFT**), redn. due to a leakage current of a switching **TFT**, and capable of preventing a redn. of the brightness of **light** emitted by an electroluminescent element are described in which one region of a source region and a drain region of a switching **TFT** is connected to an input side of an SRAM, and an output side of the SRAM and a **gate electrode** of the driver **TFT** are connected so that the SRAM stores an input digital data signal until the next digital data signal is input. Computers, video cameras, DVD players, and other electronic devices employing the displays are also described.

L23 ANSWER 19 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:328141 HCAPLUS
DN 135:68868
TI Annealing effects on the electrical characteristics of pentacene **thin film transistors**
AU Lee, Jae-Hyuk; Kim, Dae-Yop; Choi, Jong Sun; Kim, Jung-Su; Kang, Dou-Yol; Shin, Dong-Myung
CS Department of Electrical and Control Engineering, Hong-Ik University, Seoul, 121-791, S. Korea
SO Journal of the Korean Physical Society (2001), 38(3), 282-285
CODEN: JKPSDV; ISSN: 0374-4884
PB Korean Physical Society
DT Journal; General Review

LA English
AB A review with 12 refs. There is currently considerable interest in the applications of conjugated polymers, oligomers, and small mols. for thin-film electronic devices. Org. materials have potential advantages as semiconductors in field effect transistors and **light-emitting diodes**. Pentacene **thin film transistors** (**TFTs**) were fabricated on glass substrates. **Aluminum** and gold were used for the gate and the source/drain electrodes, resp. Silicon dioxide was deposited as the gate insulator by plasma enhancement CVD (PECVD) and was patterned by reactive ion etching (RIE). The semiconductor layer of pentacene was thermally evapd. in vacuum at a pressure of .apprx.10-8 Torr and at a deposition rate of 0.3 .ANG./s. The **gate electrodes** were annealed before the gate insulator layer was formed. Another annealing process was performed after the source/drain electrodes were formed. The effects of the gate metal annealing were obsd. through at. force microscopy (AFM) images of the thin films and the transfer characteristics of the **TFTs**. The **TFTs** with the annealed **gate electrode** provided better characteristics than **TFTs** with the unannealed **gate electrode**. The **TFTs** with the annealed **gate electrode** exhibited field-effect mobilities as large as 0.07 cm2/Vs and on/off current ratios larger than 107. The adverse effects of the closing annealing process on the fabricated **TFTs** are clearly revealed.
RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 20 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:707404 HCAPLUS
DN 133:275217
TI Fabrication of **thin film transistors** (**TFT**) with reduced dependence on **light** conditions
IN Battersby, Stephen J.
PA Koninklijke Philips Electronics N.V., Neth.
SO PCT Int. Appl., 17 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000059027	A1	20001005	WO 2000-EP2099	20000309
	W: JP, KR				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	EP 1086490	A1	20010328	EP 2000-925108	20000309
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI				
	US 6380009	B1	20020430	US 2000-535593	20000327
PRAI	GB 1999-7019	A	19990327		
	WO 2000-EP2099	W	20000309		

AB A method of manufg. a top-gate self-aligned **thin film transistor** involves the use of back exposure of a neg. resist using the lower source and drain electrode pattern as a photomask. A transparent amorphous silicon layer is used as the **gate electrode** layer of the **TFT** structure, and the resistance of this **gate electrode** layer is reduced by subsequent

processing. For example, a silicide layer may be formed over the **gate electrode** layer which has the added advantage of reducing the transparency of the insulated gate structure of the **TFT**, thereby reducing the dependency of the **TFT** characteristics on **light** conditions.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 21 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:580204 HCAPLUS
DN 133:185623
TI Electroluminescent display, driving substrate for it, and their manufacture
IN Yamanaka, Hideo; Yamoto, Hisayoshi; Sato, Yuichi; Yagi, Hajime
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 48 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000231119	A2	20000822	JP 1999-32250	19990210

AB The title driving substrate having a driving circuit around a display part is manufd. by the following steps: (1) forming **gate electrodes**, gate insulating films, and then a steplike gap on a surface of a substrate, (2) forming a semiconductor-contg. Sn, Pb, or Sn-Pb alloy layer with low m.p. on the substrate, (3) cooling the low-m.p. layer for graphoepitaxy of the semiconductor by using the gap as seed to form a single crystal semiconductor layer, (4) processing the semiconductor layer to form channel, source, and drain regions, and (5) forming a dual-gate **thin film transistor** (**TFT**) with the active regions, and the **TFT** forms part of the driving circuit. The title display having the driving substrate and manufg. method of the display are also claimed. High electron/hole mobility is shown in the semiconductor layer, and the driving circuit shows high performance. The electroluminescent display may be liq.-crystal display, **light-emitting** polymer display, **light-emitting diode** display, etc.

L23 ANSWER 22 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:499345 HCAPLUS
DN 133:82897
TI Fabrication of a double injection **thin film transistor**
IN Ahn, Inn-ho
PA Lg Electronics Co.,ltd., S. Korea
SO Repub. Korea, No pp. given
CODEN: KRXXFC
DT Patent
LA Korean
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
KR 9613506	B1	19961005	KR 1989-19109	19891221

AB A **thin film transistor** (**TFT**) driven by DIFET (Double Injection Field Effect Transistor) comprises a

source electrode of a **TFT** contacted to a cathode electrode of a DIFET device through a metal pad layer by the following steps: depositing a Cr or Ta metal film on a glass substrate; forming a 1st **gate electrode**, a metal pad layer and a 2nd **gate electrode**; forming a gate insulating layer on the **gate electrodes**; depositing an a-Si layer on the gate insulating layer; forming an a-Si layer on one side of the DIFET device region and on the a-Si layer of the **TFT** device region; forming a P+ a-Si layer on the other side of the DIFET device region; depositing an **Al** or Cr metal on the structure; and forming an anode electrode, a cathode electrode, a source electrode and a **diode**.

L23 ANSWER 23 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:114148 HCAPLUS
DN 132:144178
TI Optical filter for fabricating self-aligned amorphous Si **TFTs**
AU Mei, P.; Lu, J. P.; Chua, C.; Ho, J.; Wang, Y.; Boyce, J. B.
CS Xerox Palo Alto Research Center, Palo Alto, CA, USA
SO Materials Research Society Symposium Proceedings (1999), 557(Amorphous and Heterogeneous Silicon Thin Films: Fundamentals to Devices--1999), 677-682
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB Self-aligned structures for bottom-gate amorphous Si **TFTs** provide a no. of advantages, including reduced parasitic capacitance, smaller device dimensions, and improved uniformity in device performance for large-area electronics. A difficult challenge in making self-aligned **TFT** structures is the necessity of making source/drain contacts that exhibit low contact resistances and that are precisely aligned relative to the **gate electrode**. The authors describe a novel process for fabricating self-aligned amorphous Si **TFTs**. This process uses a pulsed excimer laser (308 nm) to dope or to activate dopants in a-Si to form the source/drain contacts. An important feature of the device design is an optical filter to protect the a-Si channel region from radiation damage during the 308 nm laser process. However, the optical filter allows the transmission of the UV **light** for lithog. exposure from the backside of the substrate to align the channel region with the **gate electrode**. This new process enables the fabrication of high performance self-aligned a-Si **TFTs** with poly-Si source and drain contacts.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 24 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:234088 HCAPLUS
DN 130:244562
TI Display pixels driven by silicon **thin-film transistors** and method of fabrication
IN Carey, Paul G.; Smith, Patrick M.
PA The Regents of the University of California, USA
SO PCT Int. Appl., 28 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1
PATENT NO. KIND DATE APPLICATION NO. DATE

PI	WO 9917155	A1	19990408	WO 1998-US20690	19980928
	W: JP				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 5994174	A	19991130	US 1997-940104	19970929
PRAI	US 1997-940104		19970929		

AB Display pixels driven by silicon **thin-film transistors** are fabricated on plastic substrates for use in active-matrix displays, such as flat panel displays. The process for forming the pixels involves a prior method for forming individual silicon **thin-film transistors** on low-temp. plastic substrates. Low-temp. substrates are generally considered as being incapable of withstanding sustained processing temps. greater than about 200.degree.. The pixel formation process results in a complete pixel and active matrix pixel array. A pixel (or picture element) in an active-matrix display consists of a silicon **thin-film transistor** (**TFT**) and a large electrode, which may control a liq. crystal **light** valve, an emissive material (such as a **light-emitting diode** or **LED**), or some other **light-emitting** or attenuating material. The pixels can be connected in arrays wherein rows of pixels contain common **gate electrodes** and columns of pixels contain common drain electrodes. The source electrode of each pixel **TFT** is connected to its pixel electrode and is elec. isolated from every other circuit element in the pixel array.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L23 ANSWER 25 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:14009 HCAPLUS
DN 130:74844
TI Method for making a **thin film transistor** by laser crystn. of amorphous silicon
IN Shimogaichi, Yasushi; Hayashi, Hisao
PA Sony Corporation, Japan
SO Eur. Pat. Appl., 14 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

PI	EP 886319	A2	19981223	EP 1998-111151	19980617
	EP 886319	A3	20000112		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 11017191	A2	19990122	JP 1997-178993	19970619
PRAI	JP 1997-178993		19970619		

AB In prodn. of a **thin film transistor**, a **gate electrode** is formed on an insulating substrate. A gate nitride film and a gate oxide film are formed on the **gate electrode**. A semiconductor thin film is formed on the gate oxide film. The semiconductor thin film is irradiated with laser **light** for crystn. The growth of the crystal grains in a 1st section of the semiconductor thin film lying just above the **gate electrode** is more significant than that of the crystal grains in a

2nd section of the semiconductor thin film lying in a position other than just above the **gate electrode**. An impurity is selectively doped into the 2nd section of the semiconductor thin film to form a source region and a drain region, while the 1st section of the semiconductor thin film is left without modification as a channel-forming region.

L23 ANSWER 26 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:564237 HCAPLUS
DN 129:183075
TI **Thin film transistors** fabricated on plastic substrates
IN Gates, Stephen Mcconnell
PA International Business Machines Corp., USA
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5796121	A	19980818	US 1997-823844	19970325
	JP 10270711	A2	19981009	JP 1998-69911	19980319
PRAI	US 1997-823844		19970325		

AB A **thin film transistor** incorporates a **gate electrode**, a gate insulating layer, a semiconducting channel layer deposited on top of the gate insulating layer, an insulating encapsulation layer positioned on the channel layer, a source electrode, a drain electrode, and a contact layer beneath each of the source and drain electrodes and in contact with at least the channel layer, all of which are situated on a plastic substrate. By enabling the use of plastics having low glass transition temps. as substrates, the **thin film transistors** may be used in large-area electronics such as information displays and **light**-sensitive arrays for imaging which are flexible, lighter in wt., and more impact resistant than displays fabricated on traditional glass substrates. The **thin film transistors** are useful in active matrix liq. crystal displays where the plastic substrates are transparent in the visible spectrum. The use of such plastics is enabled by means of the use of polymeric encapsulation films to coat the surfaces of the plastic substrates prior to subsequent processing and the use of novel low-temp. processes for the deposition of **thin film transistor** structures.

L23 ANSWER 27 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:344606 HCAPLUS
DN 129:35190
TI Patterns of electrically conducting polymers and their application as electrodes or electric contacts
IN Angelopoulos, Marie; Dimitrakopoulos, Christos Dimitrios; Furman, Bruce Kenneth; Graham, Teresita Ordonez; Lien, Shui-Chih Alan
PA International Business Machines Corp., USA; Angelopoulos, Marie; Dimitrakopoulos, Christos Dimitrios; Furman, Bruce Kenneth; Graham, Teresita Ordonez; Lien, Shui-Chih Alan
SO PCT Int. Appl., 113 pp.
CODEN: PIXXD2
DT Patent

LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9821755	A2	19980522	WO 1997-US20862	19971110
	WO 9821755	A3	19981008		
	W: CN, JP, KR, SG, US				
	RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	EP 953213	A2	19991103	EP 1997-949443	19971110
	R: CH, DE, ES, FR, GB, IT, LI, NL, SE, IE				
	JP 2000505249	T2	20000425	JP 1998-522863	19971110
	US 6331356	B1	20011218	US 1998-113807	19980709
PRAI	US 1996-30501P	P	19961112		
	US 1997-40129P	P	19970307		
	US 1997-40130P	P	19970307		
	US 1997-40131P	P	19970307		
	US 1997-40132P	P	19970307		
	US 1997-40159P	P	19970307		
	US 1997-40335P	P	19970307		
	US 1997-40628P	P	19970307		
	US 1989-357565	A2	19890526		
	US 1994-193926	A3	19940209		
	US 1995-476141	A2	19950607		
	WO 1997-US20862	W	19971110		
	US 1998-36458	B2	19980306		

AB Electronic devices having patterned elec. conductive polymers providing elec. connection and methods of their fabrication are described. Liq. crystal display cells are described having .gtoreq.1 of the electrodes providing a bias across the liq. crystal material formed from a patterned elec. conductive polymer. **Thin film transistors** having patterned elec. conductive polymers as source, drain, and **gate electrodes** are described. **LEDs** having anode and cathode regions formed from patterned elec. conductive polymers are described. Methods of patterning using a resist mask; patterning using a patterned metal layer; patterning the metal layer using a resist; and patterning the elec. conductive polymer directly to form electrodes and anode and cathode regions are described.

L23 ANSWER 28 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:117770 HCAPLUS
DN 128:211566
TI Junction devices based on sulfonated polyaniline
AU Narasimhan, M.; Hagler, M.; Cammarata, V.; Thakur, M.
CS Auburn University, AL, 36849, USA
SO Applied Physics Letters (1998), 72(9), 1063-1065
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English

AB Schottky **diodes** were fabricated using **aluminum** /neutralized-sulfonated-polyaniline (SPAN) junctions. I-V and C-V measurements were made, and the barrier height ([Fgr]B) and the background concn. (NB) were detd. to be 0.8 V and 4.times.1017/cm3, resp. Using these **diodes** as gate control, depletion-mode **thin-film transistors** were fabricated with a source and drain made of gold Ohmic contacts. The transistors were characterized by I-V measurements, and the carrier mobility detd. from devices operating in the

|VG|>|VDS| "linear" regime was about 0.01 cm2/V s. This high value of mobility could be attributed to the spherulitic (partially ordered) structures obsd. in the SPAN thin films. Field-effect transistors were also fabricated on SPAN films deposited on an n-doped silicon substrate acting as the **gate electrode** with a thermally grown oxide layer. A reasonably high on/off ratio (.apprx.4.times.103) was measured in these devices.

L23 ANSWER 29 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:28621 HCAPLUS
DN 128:109478
TI **Thin-film transistors** having a **silicon nitride** film coated a quartz substrate and fabrication thereof
IN Morita, Yoshikimi; Nakamura, Akira
PA Matsushita Electronics Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10004194	A2	19980106	JP 1996-155165	19960617
	JP 3201462	B2	20010820		

AB The quartz substrate for formation of the title transistor is coated on its rear surface with a hard **Si nitride** film (hardness 9) and is provided on its front surface with a polysilicon active layer, a gate insulator film, a **gate electrode**, a capacitor electrode, a signal circuit layer over a 1st interlayer insulator film over the capacitor electrode, a window-opened **light** shield film over 1st/2nd interlayer insulator films, and a transparent pixel electrode on the **light**-receiving component and the **light** shield film. The use of the hard **Si nitride** film protects the components from scratching of the substrates during manufg. and transporting.

L23 ANSWER 30 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:719755 HCAPLUS
DN 128:8830
TI liquid crystal display devices and manufacture thereof
IN Yamamoto, Kayo; Higuchi, Toyoki
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09281521	A2	19971031	JP 1996-89123	19960411

AB The manufg. process comprises the steps of: forming an anti-staggered **thin-film transistor** array; forming a **light**-shielding matrix layer having a **light**-transmitting segments underneath the **TFT**'s; and forming an etch stopper layer using a **gate electrode** as a mask in a self-aligning mode.

L23 ANSWER 31 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:682154 HCAPLUS
DN 127:365000
TI Polycrystalline semiconductor **TFT** and fabrication thereof for high ON current and high OFF withstand voltage
IN Masushige, Kunio; Kato, Naoki
PA A/G Technology Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09270516	A2	19971014	JP 1996-79047	19960401

AB The title **TFTs** comprise a glass substrate, a sublayer film, a polycryst. Si, a gate insulator film, a **gate electrode**, source/drain regions, an interlayer insulator film, source/drain electrodes, pixel electrodes, a **light** shielding film, and offset regions. The source/drain electrodes are provided each on the offset regions over the gate insulator film and interlayer insulator film. The arrangement gives the **TFTs** increased OFF withstand voltage and increased ON current.

L23 ANSWER 32 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:479308 HCAPLUS
DN 127:101866
TI Illumination device and formation of **thin-film transistors**
IN Park, Cheol-hee; Jang, Jong-seok
PA Hyundai Electronics Industries Co., Ltd., S. Korea
SO Ger. Offen., 9 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
DE 19651590	A1	19970612	DE 1996-19651590	19961211
US 6022764	A	20000208	US 1996-761961	19961209
TW 447147	B	20010721	TW 1996-85115194	19961209
GB 2308230	A1	19970618	GB 1996-25761	19961211
GB 2308230	B2	20001011		
CN 1158496	A	19970903	CN 1996-121339	19961211
CN 1079581	B	20020220		
JP 09321315	A2	19971212	JP 1996-352008	19961211
PRAI KR 1995-48282	A	19951211		

AB In prepg. a **thin-film transistor**, esp. for a liq.-crystal display, an insulating substrate having a **gate electrode** and a gate insulator layer is provided. A 1st semiconductor layer is formed on the substrate. An insulator layer is formed on the 1st semiconductor layer and the gate insulator layer as an etch stop layer. A photoresist layer is deposited on the whole surface of the structure. Predetd. regions of the photoresist layer are exposed to **light** projected through the substrate while the substrate is moved horizontally. The etch stop layer is formed by developing the exposed

photoresist layer, and the remaining photoresist layer is then removed.

L23 ANSWER 33 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:250884 HCAPLUS
DN 126:245539
TI Manufacture of **thin-film transistors**
IN Tetsu, Saori; Sakamoto, Hiromi
PA Sharp Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09051098	A2	19970218	JP 1995-199538	19950804
	US 5830776	A	19981103	US 1996-685925	19960722
PRAI	JP 1995-199538		19950804		

AB **Light**-shielding metal films (e.g., Ta) for transistors are formed on **light**-transmitting substrates, while terminals for anodization are formed from the same metals at the end of the substrates, insulator films, semiconductor layers, and gate insulator films are successively formed on the **light**-shielding films, metal films from the same metals (e.g., **Al**-Ti(1.0 wt.%)) as those of **gate electrodes** are formed on part of the terminals to elec. connect the terminals and the **gate electrodes**, and oxide films are formed on the side of the **gate electrodes** through anodization using the terminals.

L23 ANSWER 34 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:203943 HCAPLUS
DN 126:205577
TI Active matrix liquid crystal display with high opening ratio and low power consumption
IN Kaneko, Toshiteru; Ono, Kikuo; Hashimoto, Kenichi; Kizawa, Kenichi; Minemura, Tetsuo
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09026599	A2	19970128	JP 1995-177274	19950713

AB The title display uses a specified **TFT** substrate which has a **light**-shielding layer between the substrate and the **TFT** and a **light**-shielding layer around the pixels.

L23 ANSWER 35 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:102074 HCAPLUS
DN 126:179969
TI Forming a self-aligned **thin-film transistor**
IN Chen, Mei-soong
PA Industrial Technology Research Institute, Taiwan
SO U.S., 7 pp.
CODEN: USXXAM

DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5597747	A	19970128	US 1995-572809	19951215

AB A substrate comprising material that is transparent to the radiation used to activate a photoresist is selected. A **gate electrode** is formed on 1 surface of the substrate. Then an insulating layer, a doped semiconductor layer, and a coating of neg. photoresist are deposited. The photoresist is then exposed, but the activating radiation is directed to it through the lower surface of the substrate. This results in a mask that allows a gap to be etched in the doped semiconductor that is perfectly aligned with the **gate electrode**. The structure includes a layer of amorphous Si together with a suitable protective layer and is completed by a conductive layer that is patterned to form connections to other parts of the circuit. The method depends on the transparency of Si relative to the metal so the wavelength of the **light** used to expose the photoresist must be taken into account. The **TFT** can be used in a liq.-crystal display.

L23 ANSWER 36 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:97053 HCAPLUS
DN 126:111950
TI Fabrication of LDD **thin-film transistors** by a single doping
IN Sadabetsuto, Hiroyasu
PA Casio Computer Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08293612	A2	19961105	JP 1995-123243	19950424

AB The process involves forming a **gate electrode** on an insulative photo-transmissive substrate, forming a transparent gate insulator film over the **gate electrode** on the substrate, forming a photo-transmissive semiconductor thin-film on the gate insulator film, forming a dope-controlling thin-film on the semiconductor thin-film, coating a p-type 1st photoresist on the dope-controlling thin-film, patterning the 1st photoresist in self-alignment to the **gate electrode** by **light** -exposing from the rear side of the substrate, patterning the dope-controlling thin-film in self-alignment over the 1st photoresist mask, coating a 2nd photoresist over a dope-controlling thin-film on a semiconductor thin film, exposing over the 2nd photoresist from the rear side of the substrate, and doping over the 2nd photoresist to give source/drain regions and a lightly-doped regions. The process provides the source/drain regions and LDD-forming lightly-doped regions in a single doping without use of masks.

L23 ANSWER 37 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:715535 HCAPLUS
DN 125:345174

TI Manufacture of polycrystalline silicon **thin film transistor**
IN Kashimoto, Noboru
PA Toshiba Electronic Eng, Japan; Tokyo Shibaura Electric Co
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08250736	A2	19960927	JP 1995-49491	19950309

PI JP 08250736 A2 19960927 JP 1995-49491 19950309

AB The manuf. involves the following steps; (1) successively forming an amorphous Si layer and a Si oxide film on an insulating substrate, (2) forming a **gate electrode** mad of a transparent material, (3) doping an impurity ion into the amorphous Si layer of a region corresponding to a source- and drain region, and (4) irradiating a **light** to the amorphous Si layer through the Si oxide film for crystg. the amorphous Si layer to give a polycryst. Si layer, and for activating the impurity-doped source- and drain regions to form an active layer. The manuf. involves the following steps; (1) successively forming a **gate electrode** made of a transparent material, and an amorphous Si layer on a transparent insulating substrate, (2) forming a gate insulating film made of a Si oxide film or a transparent insulating film, (3)irradiating a **light** to the amorphous Si layer through the gate insulating film (from the transparent substrate side) for crystg. the amorphous Si layer to form a polycryst. Si layer, and for activating an impurity-doped source- and drain regions to form an active layer. The method enables forming a Si oxide film at .ltoreq.450.degree. on a transparent insulating substrate made of a glass substrate of relatively low m.p., and the manuf. is applicable for liq. crystal display devices and image sensor.

L23 ANSWER 38 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:644791 HCAPLUS
DN 126:53285
TI Low resistivity **Al**-RE (RE = La, Pr, and Nd) alloy thin films with high thermal stability for **thin-film-transistor** interconnects
AU Takayama, Shinji; Tsutsui, Naganori
CS Dep. Electrical Eng., Hosei Univ., Tokyo, 184, Japan
SO Journal of Vacuum Science & Technology, B: Microelectronics and Nanometer Structures (1996), 14(5), 3257-3262
CODEN: JVTBD9; ISSN: 0734-211X
PB American Institute of Physics
DT Journal
LA English
AB The addn. of **light** rare-earth (RE) metal elements (La, Pr, and Nd) to **Al** thin films with about 2-7 at. % markedly decreases the grain size of the **Al** matrix more than 50% compared with those of pure **Al**. Such addn. largely suppresses growth of thermal defects of hillocks and whiskers at high temps. (350-450.degree.C). A large no. of fine metallic compds. of Al11RE3 and/or Al3RE (RE = La, Pr, and Nd) were segregated in an **Al** matrix, mostly at grain boundaries, after annealing at 350.degree.C. The resistivities of the films after annealing at the above temps. show low values of less than 6 .mu..OMEGA. cm compared with those of current **thin-film**

-transistor liq.-crystal displays **gate electrode** materials (more than about 15 .mu..OMEGA. cm), without the salient formation of hillocks or whiskers on the surfaces.

L23 ANSWER 39 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:508784 HCAPLUS
DN 125:156200
TI Manufacture of semiconductor device
IN Yamazaki, Shunpei; Kusumoto, Naoto; Teramoto, Satoshi
PA Handotai Energy Kenkyusho, Japan
SO Jpn. Kokai Tokkyo Koho, 13 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08139020	A2	19960531	JP 1995-132901	19950506
	US 5972105	A	19991026	US 1995-528407	19950914
	CN 1129850	A	19960828	CN 1995-115160	19950915
	CN 1078384	B	20020123		
PRAI	JP 1994-248791	A1	19940915		
	JP 1994-248792	A	19940915		
	JP 1995-132901	A	19950506		
	JP 1995-132902	A	19950506		

AB The manuf. comprises these steps; (1) forming a 1st a-Si film (A) on an insulating surface of a substrate, (2) contacting A with a metal promoting a-Si crystn., (3) annealing to crystallize A, (4) patterning the crystd. A to form a layer to be a crystal-nucleation layer (B), (5) forming a 2nd a-Si film (C) covering B, (6) forming a crystal-grain boundary-free region in C by crystal growth from B, and (7) forming an active layer from the crystal boundary-free region. The step (6) may be performed by annealing, preferably at 450-600.degree., with laser- or a intense-**light** irradn. The metal may be Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, and/or Au. The manuf. provides an improved **thin-film transistor** with a large ON-elec. c. and less drift of threshold voltage.

L23 ANSWER 40 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:505930 HCAPLUS
DN 125:156224
TI Manufacture of semiconductor device for **TFT** in liquid crystal display
IN Tsuboi, Nobuyuki; Hirose, Takashi; Kobayashi, Ikunori; Tamura, Tatsuhiko
PA Matsushita Electric Ind Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08172200	A2	19960702	JP 1994-316590	19941220

AB The method involves the following steps: (1) forming a **gate electrode** on a transparent substrate; (2) depositing the 1st insulator layer, a semiconductor layer, and the 2nd insulator layer; (3) selectively etching the 2nd insulator layer; (4) depositing a

dopant-contg. semiconductor layer on the whole surface; (5) expanding the dopant-contg. semiconductor layer and the semiconductor layer into the pixel electrode region of the **TFT**; (6) selectively forming source/drain electrodes; (7) depositing a transparent conductive film on the whole surface; and (8) etching the transparent conductive film by using a photoresist pattern, whose pattern is formed by using the **gate electrode** and the source electrode as a mask and exposing a photoresist film to the **light** streaming through the back side of the transparent substrate, to form a pixel electrode. The dopant-contg. semiconductor layer may comprise microcrystal Si.

L23 ANSWER 41 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:409687 HCAPLUS
DN 125:73852
TI Manufacture of **TFTs** (**thin film transistor**)
IN Myagawa, Tatsuya
PA Casio Computer Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08088372	A2	19960402	JP 1994-248737	19940916

AB The process includes: (1) after forming a **gate electrode** on a transparent substrate, successively forming a gate oxide film, a semiconductor film, a thin cap film, and a transparent blocking film; (2) self-aligning a resist pattern by spreading a resist film, exposing it to the **light** from the back side of the transparent substrate, and developing it; (3) by using the resist pattern as a mask, selectively etching the blocking film to form a mask; and (4) by using the mask, implanting ions into the semiconductor film to form source/drain regions. The thin cap film may be a SiO2 film, and the blocking film may be an ITO (indium **tin** oxide) film. In the step 3, the blocking film may be etched by an aq. soln. of HCl and HNO3, when the thin cap film acts as an etching stopper. The title manuf. is characterized by the thin cap film. The semiconductor film may be an amorphous Si film, which is transformed to a poly-Si film after the step 4 by annealing.

L23 ANSWER 42 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:251192 HCAPLUS
DN 124:303768
TI Nonphotosensitive, vertically redundant two-channel a-Si:H **thin film transistor**
AU Kuo, Yue
CS IBM T. J. Watson Res. Cent., Yorktown Heights, NY, 10598, USA
SO Journal of the Electrochemical Society (1996), 143(4), 1469-71
CODEN: JESOAN; ISSN: 0013-4651
PB Electrochemical Society
DT Journal
LA English
AB An amorphous silicon a-Si:H **thin film transistor** (**TFT**), which has (i) two sep. channels vertically stacked, (ii) two **gate electrodes**, i.e., one on the top and the other one at the bottom, and (iii) a self-aligned

source/drain to bottom gate structure, is presented and studied. This **TFT** is not sensitive to **light** illumination because the channels are enclosed by two opaque **gate electrodes**. It has an Ioff less than 10-12 A, an Ion/Ioff ratio greater than 106, and a subthreshold slope of 0.42 V/decade. When both **gate electrodes** are driven, the value of Ion is higher than the sum of the two sep. values of Ion corresponding to each **gate electrode** driven individually. The high performance of the two-channel **TFT** is due to the field enhancement from both the top and the bottom gates.

L23 ANSWER 43 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:197200 HCAPLUS
DN 124:248053
TI **Thin film transistor**, its manufacture, and liquid crystal display device using it
IN Asaba, Tetsuro
PA Canon Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08018064	A2	19960119	JP 1995-115320	19950418
PRAI	JP 1994-109100		19940426		

AB In the field-effect **thin film transistor** (**TFT**), successively comprising a transparent substrate, a **gate electrode**, a gate-insulating layer, and a semiconductor layer contg. a channel, a source, and a drain regions, the **gate electrode** comprises Si - metal silicide bilayer, and the gate-insulating film of which the part contacting with the channel consists of SiO2 . The **gate electrode** layer may be a triple layer of Si - metal silicide - Si. The metal silicide layer may be **W** silicide. Optionally, the semiconductor layer may be coated with a 2nd **gate electrode** of Si layer, via a 2nd gate-insulating film of which the part contacting with the channel being SiO2 . The manuf. comprises these steps; forming the **gate electrode** on the substrate, oxidizing (and optionally annealing) the surface, depositing the semiconductor layer to form the channel, the source, and the drain regions. The liq. crystal display device includes the **TFT** as a switching device of active matrix-type substrate. The **TFT** has a good **light**-blocking property of the multilayer **gate electrode**, and provides improved switching characteristics with the liq. crystal display device.

L23 ANSWER 44 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:1006993 HCAPLUS
DN 124:104087
TI Manufacture of bottom gate-type **thin film transistor**
IN Morosawa, Katsuhiko; Shimomaki, Shinichi
PA Casio Computer Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent

LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 07273344	A2	19951020	JP 1994-83699	19940331

AB A bottom gate-type **thin film transistor** is manufd. by a process including following successive steps: (1) successively forming a thermal insulator layer (A) and a resist layer (B) on a semiconductor layer (C), which is assocd. with a gate insulator layer on a **gate electrode**, (2) patterning B through the electrode as mask by photolithog., (3) patterning A through B, (4) implanting impurities into C through A and/or B, and (5) annealing from A side.

L23 ANSWER 45 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:896675 HCAPLUS
DN 123:327812
TI Manufacture of reverse-stagger **thin-film transistors**
IN Myagawa, Tatsuya
PA Casio Computer Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 07183531	A2	19950721	JP 1993-346011	19931224

AB The process includes the steps: (1) forming **light**-shielding masks at both sides of **gate electrodes** (formed on transparent substrates) at distance; (2) successively forming gate insulator films and semiconductor films; (3) forming resists and developing them after exposure using the masks of the **gate electrodes** and **light**-shielding masks; (4) implanting low-concn. dopants in the semiconductor films using the masks of residual resists; (5) removing the resists above the **light**-shieding masks; and (6) implanting high-concn. dopants of opposite cond. in the semiconductor films using the resists above the **gate electrodes**. The process includes the further steps: (7) forming etching holes in the semiconductor films and gate insulator films corresponding to the **light**-shielding masks; (8) etching the **light**-shielding masks through the holes; (9) depositing the resist solns. on the semiconductor films; and (10) developing the resists after exposure with the **gate electrodes** as masks to form resist films only above the **gate electrodes**. The process forms low-concn. doped regions of uniform width between the high-concn. doped regions and the channel-forming regions in self-alignment.

L23 ANSWER 46 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:795398 HCAPLUS
DN 123:244359
TI Making a self-aligned amorphous-silicon **thin-film transistor**
IN Wu, Biing Seng
PA Industrial Technology Research Institute, Taiwan

SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5441905	A	19950815	US 1993-52519	19930429

AB To manuf. a **TFT** for an active-matrix liq.-crystal display having self-aligned source and drain electrodes to minimize the stray capacitance between the gate and the source/drain electrodes, the source and drain electrodes are obtained by exposing a neg. photoresist on top of the transistor by incident **light** from the back of the transparent substrate, using the **gate electrode** as a mask.

L23 ANSWER 47 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:507931 HCAPLUS
DN 122:253863
TI **Thin-film transistors**
IN Ishiguro, Kenichi
PA Sharp Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 06260503	A2	19940916	JP 1993-44175	19930304

AB SiNx films are formed on insulator substrates, neg. resists are deposited on the films, and are exposed to UV **light** from the bottom side of the substrates with **gate electrodes**, gate insulator films, and semiconductor films as masks, unexposed part of the resists are removed through development, interlayer insulator films are formed, and Mo films are formed and patterned into source and drain electrodes.

L23 ANSWER 48 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:462881 HCAPLUS
DN 122:227029
TI Patterning of Cr film and manufacture of **TFT** (**thin-film transistor**) matrix
IN Kosugi, Kyohisa; Watabe, Junichi; Shiroki, Ikuo
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 07020493	A2	19950124	JP 1993-151708	19930623

AB Patterning of Cr films involves the following steps; (1) forming a Cr film on a substrate, (2) forming a metal film A (preferably, **Al** or Ti), (3) forming a resist film on A, (4) patterning of the resist film by **light**-exposure, developing, and etching using the patterned resist film as a mask. In manuf. of a **TFT** matrix comprising a transparent insulating substrate, multiple **TFT** (contg. a

gate electrode, an interlayer insulating film, a semiconductor film, source and drain electrodes), and bus lines. .

L23 ANSWER 49 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:268821 HCAPLUS
DN 122:44320
TI **Thin-film transistor** element with stagger-structure
IN Ando, Masahiko; Kizawa, Kenichi
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 06275831	A2	19940930	JP 1993-58348	19930318

AB The element comprises a substrate successively laminated with a source and a drain electrodes, a pair of doped semiconductor layers, a semiconductor-activating layer across the pair of semiconductor layers, an elec. insulating layer contg. a **light**-absorbent with absorption coeff. .gtoreq.10-4 at 500 nm wavelength, and a **gate electrode**. The **light**-absorbent may be PrMnO3, As2S3, As2Se3, Ge, a-SixCl-x:H, Sb2S3, CdTe, CdSe, or PbCdTe:In. The element showed decreased photoelec. current.

L23 ANSWER 50 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:669723 HCAPLUS
DN 121:269723
TI Preparation of gate and display electrodes for **thin-film transistors**
IN Oota, Norio
PA Dainippon Printing Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 06097445	A2	19940408	JP 1992-247863	19920917

AB Transparent electrodes (e.g., ITO) are deposited on **light**-transmitting substrates, metal films (e.g., Ti) formed, and the film laminates photoetched to simultaneously create gate and display electrode patterns. The metal films are etched away with the gate insulator film patterns as masks.

L23 ANSWER 51 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:619361 HCAPLUS
DN 121:219361
TI **Thin-film transistors** for liquid-crystal display devices, and their manufacture
PA Casio Computer Co., Ltd., Japan; Oki Electric Industry Co., Ltd.
SO Neth. Appl., 30 pp.
CODEN: NAXXAN
DT Patent

LA Dutch
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	NL 9302256	A	19940718	NL 1993-2256	19931224
	NL 194380	B	20011001		
	NL 194380	C	20020204		
	JP 06202147	A2	19940722	JP 1992-347601	19921228
	JP 06202148	A2	19940722	JP 1992-347602	19921228
	US 5539551	A	19960723	US 1993-168644	19931216
PRAI	JP 1992-347601	A	19921228		
	JP 1992-347602	A	19921228		

AB The liq.-crystal display devices comprise a no. of address circuit layers, a no. of data circuit layers crossing the address circuit layers, a no. of **thin-film transistors** equipped with a **gate electrode**, a semiconductor layer, a feed electrode, and a discharge electrode. The **gate electrode** of each row of **thin-film transistors** is connected to the corresponding address circuit layers, and one of the feed electrodes and the discharge electrode of each **thin-film transistor** is connected to the corresponding no. of data circuit layers. Each of the feed electrode and discharge electrode of each **thin-film transistor** is provided with a 1st layer, formed on the semiconductor layer and serving as an ohmic layer, a 2nd layer, formed on the 1st layer and essentially consisting of a conductive material and serving primary signal circuit layer, and a 3rd layer, formed on the 2nd layer, and being liq.-impervious and serving battery reaction-preventing layer, and display electrodes arranged in a matrix and each of them elec. connected to with the other of the feed electrode and discharge electrode of the corresponding one of the **thin-film transistor**. The **thin-film transistors** are manufd. by forming the **gate electrode** on a substrate, forming an insulating film on the **gate electrode**, forming a semiconductor layer on the insulating layer at a position corresponding the the **gate electrode**, forming a 1st layer, serving as barrier layer, on the semiconductor layer, forming a conductive 2nd layer on the 1st layer, forming a liq.-impervious 3rd layer on the 2nd layer, forming a resist film on the 3rd layer, exposing the film to **light** and developing the film using a soln. to form an etching mask, in which the 3rd layer prevents penetration of the soln. through the 2nd layer, and forming a feed electrode and a discharge electrode by structuring at least the 1st and 2nd layer with the etching mask.

L23 ANSWER 52 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:593402 HCAPLUS
DN 121:193402
TI Fabrication of **thin-film transistors**
IN Shiraishi, Hitoshi
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI JP 06029318 A2 19940204 JP 1992-179519 19920707
JP 2838943 B2 19981216
AB Title fabrication involves forming a **Si nitride** film and an a-Si film successively on a glass substrate over a **gate electrode**, coating a photoresist film over the a-Si film, patterning an n+-a-Si film by exposing **light** on the rear side of the glass substrate, forming a channel region by lifting off, forming a Cr film as a **gate electrode** in aligning to the photoresist film which is formed on the channel region, and forming source and drain electrodes by lifting off. Title fabrication avoids dry etching in formation of the channel region so that damage caused by plasma treatment on the region is prevented.

L23 ANSWER 53 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:313473 HCAPLUS
DN 120:313473
TI Manufacture of **thin-film transistors**
IN Ichimura, Teruhiko; Murata, Juji; Iida, Heiji
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05267343	A2	19931015	JP 1992-63814	19920319

AB Manuf. of a **thin-film transistor** includes: (a) forming a **gate electrode** on a transparent insulator substrate; (b) successively forming a gate insulator film, active semiconductor layer, channel-protection film, and a **light**-transmitting elec.-conductive film; (c) patterning the **light**-transmitting elec.-conductive film and the channel-protection film in self-alignment with the **gate electrode**; (d) forming an electrode contact layer and an electrode material layer; (e) patterning the electrode material layer, electrode contact layer, and the active semiconductor layer, forming source and drain electrodes connected through the **light**-transmitting elec.-conductive film on the channel-protection film, as well as insulating the device; and (f) removing part of the **light**-transmitting elec.-conductive film on the channel-protection film to disconnect the source and drain electrodes.

L23 ANSWER 54 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:259096 HCAPLUS
DN 120:259096
TI Manufacture of **thin-film transistors** for LCDs
IN Nagahiro, Norio; Tanaka, Tsutomu; Yanai, Kenichi
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05175233	A2	19930713	JP 1991-343501	19911225

JP 3105606 B2 20001106

AB The process contains: (a) selectively forming a **light**-shielding film on a transparent substrate, and forming an insulator film on the whole surface; (b) forming a 1st patterning film by photolithog. using the **light**-shielding film as a mask in a channel-layer-intended region on the insulation film, and forming a 2nd patterning film by photolithog. using a 1st exposure mask in the regions on the insulator film, where pixel electrodes and source/drain electrodes are not intended; (c) forming a **light**-transmitting 1st elec.-conductive film (e.g., ITO/a-Si) on the insulator film across the 1st and 2nd patterning films; (d) removing the 1st and 2nd patterning film to form, by liftoff, pixel and source/drain electrodes from the elec.-conductive film; (e) forming a semiconductor layer and a 1st gate insulator film to bridge the source/drain electrodes, and forming a drain bus line connected with the drain electrode; (f) forming a 2nd gate insulator film and a **light**-transmitting 2nd elec.-conductive film on the 1st gate insulator film; (g) forming a 3rd patterning film on the 2nd elec.-conductive film by photolithog. using the **light**-shielding film as a mask, and forming a 4th patterning film by photolithog. using a 2nd exposure mask on the 2nd elec.-conductive film in a region where a gate bus line is intended; and (h) etching the 2nd elec.-conductive film with the 3rd and 4th patterning films as a mask to form a **gate electrode** and a gate bus line connected with it. The source/drain electrodes and the **gate electrode** are selfaligned, decreasing floating capacitance between the electrodes.

L23 ANSWER 55 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:257551 HCAPLUS
DN 120:257551
TI **Thin-film transistor** optical sensor
IN Kaneko, Yoshuki; Yamaguchi, Muneaki; Tsutsui, Ken
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05235398	A2	19930910	JP 1992-36001	19920224

AB The sensor consists of a **gate electrode**, a gate insulating film, a semiconductor layer, a source and a drain electrode, and a transparent gate auxiliary electrode on the side of the semiconductor opposite to the **gate electrode** as sepd. from the semiconductor layer by a 2nd insulating film, for incidence of a **light** from the side of the auxiliary electrode and driving of the sensor by fixing the potential of the auxiliary electrode. The potential of the auxiliary electrode is selected such that no charge is induced on the interface between the 2nd insulating film and the semiconductor layer and dark current is minimized.

L23 ANSWER 56 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:179560 HCAPLUS
DN 120:179560
TI The effects of **light** and electrical stress on asymmetric amorphous silicon **TFT**
AU Oh, C.H.; Chung, I.J.; Kim, W.Y.; Hwang, J.R.; Lee, S.K.; Kim, Y.S.; Park,

J.S.; Han, M.K.
CS An-Yang Res. Lab., GoldStar Co., An-Yang, 430-080, S. Korea
SO Materials Research Society Symposium Proceedings (1993), 284(Amorphous Insulating Thin Films), 419-24
CODEN: MRSPDH; ISSN: 0272-9172
DT Journal
LA English
AB The asym. amorphous Si **thin film transistors** are fabricated and exposed to various stress environments. A visible **light** illumination of 200,000 lx and gate bias of 30 V are applied to both asym. and widely used sym. a-Si **TFT**'s. The leakage current of asym. structure, where only one electrode is fully overlapped by **gate electrode**, is much less than that of sym. 1. The visible **light** illumination as well as gate bias stress do not degrade the leakage current of the asym. a-Si **TFT**'s, while the leakage current in the sym. **TFT**'s are increased considerably due to the stress. The degree of degrdn. in the threshold voltage, the field effect mobility and the subthreshold slope of asym. **TFT**'s are relatively much less than that of conventional sym. **TFT**'s.

L23 ANSWER 57 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:438849 HCAPLUS
DN 119:38849
TI Etching method and its use in manufacturing **thin-film transistors**
IN Watanabe, Kazuhiro; Dejima, Yoshio; Nagahiro, Norio; Soeda, Shinichi; Sato, Kiyotake
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 04357832	A2	19921210	JP 1991-132497	19910604

AB The title etching method involves depositing an **Al** layer on a Ti layer and patterning the **Al** layer to a specified shape by using a resist mask, followed by forming a protective film, which on the side wall of the **Al** layer, is resistant to an etchant comprising Cl or Cl-contg. compd.. The title manuf. involves (1) forming a **gate electrode** and a Ti gate bus on a substrate; (2) successively forming 1st Si3N4 insulating layer, 1st amorphous Si layer, and a 2nd insulating layer, (3) forming a resist layer corresponding to the **gate electrode** on the 2nd insulating layer, (4) selectively etching the 2nd insulating layer exposed on the resist layer, to expose the 1st amorphous Si, (5) successively depositing doped amorphous Si layer and ti layer and **Al** layer to cover the exposed 1st amorphous Si layers and (6) using the title etching method.

L23 ANSWER 58 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:181467 HCAPLUS
DN 118:181467
TI Manufacture of **thin-film transistor**
IN Yudasaka, Kazuo
PA Seiko Epson Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.

CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 04290443	A2	19921015	JP 1991-54702	19910319

AB The title process comprises: (1) forming an amorphous Si layer .ltoreq. 2000 .ANG. thick at an insulating film for the subsequent formation of a source, a drain, and a channel; (2) forming a 1st polysilicon film by lamp annealing the amorphous Si film with a **light** having wavelength 350-500 nm; (3) forming a gate insulating film; (4) forming a 2nd polysilicon film for the **gate electrode** formation; (5) ion implanting the source, drain, and **gate electrode** regions to the dopant concn. of .gtoreq. 1 .times. 1015/cm2; (6) activating the implanted dopants by lamp annealing with a **light** having wavelength 350-500 nm; (7) forming an interlayer insulating film; and (8) forming a wiring such as **Al**. The amorphous Si film can be obtained by low-pressure CVD using a silane gas. **Thin-film transistors** having uniform elec. characteristics can can be obtained with high throughput on large substrates.

L23 ANSWER 59 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:14109 HCAPLUS
DN 118:14109
TI **Thin-film transistor**
IN Hiramoto, Hiroyuki; Hayakawa, Koji; Shinno, Chikashi
PA Stanley Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 04119331	A2	19920420	JP 1990-239480	19900910

AB The title transistor comprises (1) a semiconductor channel layer on a gate insulator, (2) source and drain electrodes connected to the channel region, (3) a transparent electrode which is connected to the drain electrode and is formed on the gate insulator layer, (4) a 1st protective layer on the **gate electrode**, (5) a **light** -shielding layer covering the channel region, and (6) a liq. crystal orientation film formed on the 1st layer via a 2nd protective layer which is made of a material different from the 1st layer and has a good wettability with resp. to the liq. crystal film. The bonding of the liq. crystal film is improved. The transistor is useful in a liq.-crystal display device.

L23 ANSWER 60 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:624599 HCAPLUS
DN 117:224599
TI **Thin-film transistor** and its manufacture
IN Hiramoto, Hiroyuki
PA Stanley Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent

LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 04132263	A2	19920506	JP 1990-253965	19900921

AB The transistor comprises (1) a gate insulator layer formed on a glass substrate via a **gate electrode** layer; (2) an amorphous Si semiconductor layer on the gate insulator layer; (3) a pair of source and drain electrodes on the semiconductor layer; (4) a transparent electrode layer on the drain electrode and gate insulator layer; (5) a protective layer on the semiconductor layer and electrodes; and (6) an amorphous Si **light**-shield layer on the protective layer. Specifically, the protective layer may comprise **Si nitride**.

L23 ANSWER 61 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:623228 HCAPLUS
DN 117:223228
TI Manufacture of **thin-film transistor**
IN Toko, Yasuo
PA Stanley Denki K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 04111322	A2	19920413	JP 1990-229111	19900830

AB A method for manufg. a **thin-film transistor** by successively depositing a **gate electrode** layer, gate insulator film, semiconductor layer, source-drain electrode layer, channel-coating film, and channel-shielding film on a transparent insulator substrate involves forming imaging electrodes integral with the drain electrodes simultaneously with the formation of sources-drain electrode layers on the semiconductor layer and substrate. Specifically, the **light**-shielding film comprises a conductor and partially makes contact with the tip of the **gate electrode**. The transistor is useful in an active-matrix circuit of a display device.

L23 ANSWER 62 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:562231 HCAPLUS
DN 117:162231
TI Manufacture of **thin-film transistors**
IN Kobayashi, Kenichi; Hirota, Masanori
PA Fuji Xerox K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 04075350	A2	19920310	JP 1990-188093	19900718

AB Manuf. of a **thin-film transistor** includes: (a) forming a channel-protection layer, whose shape corresponds to that of a **gate electrode**, with the use of a 1st resist

pattern, and depositing an ohmic contact layer and a transparent elec. conductive film; (b) forming an image-reversal resist film; (c) forming a 2nd resist pattern by photolithog. on source and drain electrodes; (d) applying **light** from the substrate bottom; (e) baking the image-reversal resist film; (f) applying **light** from the substrate top; (g) developing the image-reversal resist film to remove the resist on the channel-protective layer, forming a 3rd resist pattern; and (h) etching the ohmic contact layer, the transparent elec. conductive film, and the semiconductor active layer with the 3rd resist pattern as a mask.

L23 ANSWER 63 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:459058 HCAPLUS
DN 117:59058
TI **Thin-film transistor** array
IN Tsunohashi, Takeshi; Goto, Kazuhito; Namikawa, Akira; Tatsumi, Motoshige
PA Nitto Denko Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 03203245	A2	19910904	JP 1989-343763	19891228

AB The title array comprises a transparent polymer film substrate, a thin film of SiOx (x = 1-2), ZrO2, Al2O3, Ta2O5, SiC, TiC, **Si nitride**, and/or **TiN** on 1 side of (or both sides of) the substrate, on the thin film or on the other side of the substrate, a **gate electrode**, a gate insulating film, a semiconductor layer, and source drain electrodes. The array is useful as a liq.-crystal display panel. By using the elastic substrate, the panel can have a curvature to decrease the reflection **lights**.

L23 ANSWER 64 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:14260 HCAPLUS
DN 116:14260
TI Manufacture of arrays of **thin-film transistors** for display devices
IN Nakatani, Norio; Sasaki, Terushi; Yoshizako, Keizo
PA Sanyo Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 03192728	A2	19910822	JP 1989-333971	19891221

AB The process includes: (a) forming .gtoreq.2 gate interconnections contg. a 1st-metal (e.g., Cr) **gate electrode** on a **light** -transmitting substrate; (b) forming a gate insulator film and a semiconductor film on the substrate; (c) forming a resist, and patterning the semiconductor film with the resist as a mask; and (d) forming a transparent elec. conductive film (e.g., In-Sn-O), and patterning the film with a resist as a mask to sep. in 1 direction, where the resist has a reversed pattern of the gate interconnections. The steps are followed by:

(e) forming a resist which has a reversed pattern of drain interconnections and patterning the elec. conductive film with the resist as a mask to form a large no. of display electrodes; (f) depositing a 2nd metal (e.g., Ti) on the whole surface, and forming drain interconnections from the 2nd metal by lift-off; and (g) forming a large no. of source interconnections from a 3rd metal (e.g., **Al**).

L23 ANSWER 65 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1991:197880 HCAPLUS
DN 114:197880
TI Fabrication of **thin-film transistors**
IN Nakatani, Norio
PA Sanyo Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 02273935	A2	19901108	JP 1989-95832	19890414

AB The process follows the steps of (a) forming a **gate electrode** and gate interconnection from a nontransparent 1st metal on a transparent insulation substrate; (b) successively forming a transparent gate insulator film and a semiconductor film on the metal, and making the latter in an island shape; and (c) depositing a transparent elec.-conductive film on the whole surface. The steps are further followed by (d) forming a resist layer having a reversed pattern to that of the metal film by applying **light** from the bottom side; (e) removing the elec.-conductive film with the resist layer as a mask; (f) photo-etching the elec.-conductive film by using a photomask to form source, drain, and display electrodes; and (g) depositing a 2nd metal, and forming a drain interconnection.

L23 ANSWER 66 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:170211 HCAPLUS
DN 112:170211
TI Amorphous silicon phototransistors
AU Kaneko, Yoshiyuki; Koike, Norio; Tsutsui, Ken; Tsukada, Toshihisa
CS Cent. Res. Lab., Hitachi, Ltd., Kokubunji, 185, Japan
SO Appl. Phys. Lett. (1990), 56(7), 650-2
CODEN: APPLAB; ISSN: 0003-6951
DT Journal
LA English
AB An amorphous Si field-effect phototransistor was fabricated using a processing technol. compatible with conventional amorphous Si-**Si nitride thin-film transistors**. The phototransistor has an offset structure between the source and **gate electrodes**, where **light** is absorbed to produce a photocurrent. In an electron accumulation mode, the photocurrent is greater than the dark current by 3 orders of magnitude. In addn., the phototransistor was output characteristics showing good satn. Typical photoconductive gain of this satn. current is 17.

L23 ANSWER 67 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1987:187544 HCAPLUS
DN 106:187544

TI **Thin-film transistor**
IN Tsutsui, Ken; Kaneko, Yoshiyuki; Oritsuki, Ryoji; Tsukada, Toshihisa
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 2 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 62020375	A2	19870128	JP 1985-158173	19850719

AB A method for fabricating a **thin-film transistor** consisting of a **gate electrode**, gate insulator, and amorphous Si film on a transparent substrate involves the following steps: (1) casting the amorphous Si film with a resist sensitive to a wavelength >4800 .ANG.; and (2) exposing the resist from the backside of the substrate with a **light** source (e.g., **W** lamp) having the wavelength 4800-7000 .ANG., using the **gate electrode** as a mask. The efficiency of the backside exposure is improved.

L23 ANSWER 68 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1980:560134 HCAPLUS
DN 93:160134
TI **Thin film transistor**
PA Westinghouse Electric Corp., USA
SO Brit., 10 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI GB 1565551	A	19800423	GB 1976-33948	19770106

AB The manuf. is described of **thin-film transistors** with improved transconductance and high-voltage performance and reduced charge trapping, the transistors being particularly suitable for large-area flat electroluminescent display panels. The transistors are vapor deposited in successive steps on a glass substrate. An **Al** gate layer is deposited on the substrate and an **Al** oxide insulating layer is deposited over it, the gate extending beyond the insulating layer. A CdSe semiconductive layer is deposited on the insulating layer and overlays part of the gate. The CdSe layer contains sufficient In to stabilize the device. The CdSe layer forms a channel between the source and drain contacts which is .apprx.2-2.5 mils long for electroluminescent displays. Source and drain contacts overlap opposite sides of the channel and each comprises a 1000-.ANG.-thick Cu layer on a 100-.ANG.-thick In layer. A 2nd **Al** oxide insulating layer is disposed over the source and drain contacts and a 2nd **Al gate electrode** is positioned on the 2nd insulating layer.

L23 ANSWER 69 OF 69 HCAPLUS COPYRIGHT 2002 ACS
AN 1971:148101 HCAPLUS
DN 74:148101
TI Tellurium **thin film transistors**
AU Kimura, Masayoshi; Okuyama, Katsuro; Kumagai, Yasuji

CS Fac. Eng., Yamagata Univ., Yonezawa, Japan
SO Yamagata Daigaku Kiyo, Kogaku (1969), 10(2), 651-62
CODEN: YDKKAR
DT Journal
LA Japanese
AB The voltage-current characteristics of coplanar **diodes** made of deposited Te and metal films were measured. Good ohmic contacts to Te films could be made with Co, Ni, Au, and In, which seemed to be suitable as source-drain electrodes, while **Al** or Cr produced a blocking contact. The Hall mobility of Te films depended on film thickness in such a way that the mobility for a film 200 A thick was .apprx.2 cm2/V-sec increased to 20 cm2/V-sec for a thickness of 2000 A. The temp. dependence of Hall mobility at <70.degree. indicated the ion scattering mechanism to be dominant. An increase in Hall mobility on application of the gate field was obsd., as seen in the case of CdSe films. The Te **thin -film transistors** were fabricated on glass substrates by deposition of Au, Co, or **Al** as a source-drain electrode, a 170-180-.ANG. Te layer, a SiO insulator layer 1000 A thick, and finally **Al** metal as a **gate electrode**. For Au and Co electrodes, the mutual conductance of Te **thin-film transistors** was 200-1880 .mu.mho, while a very small value as well as large hysteresis was obsd. when **Al** was used as the source-drain electrode.